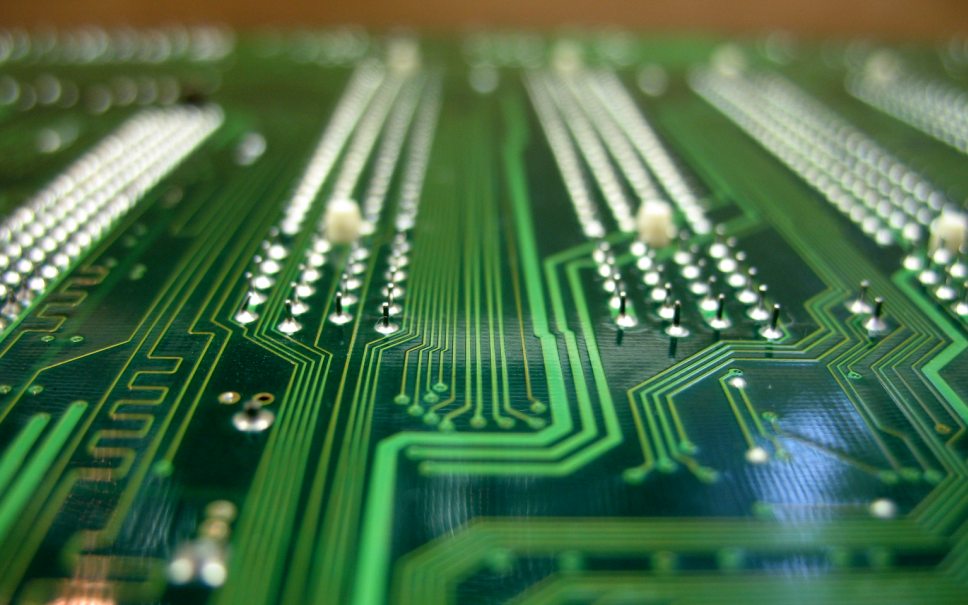
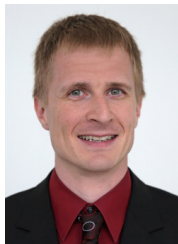




In-Memory Database Systems

Jens Teubner · TU Dortmund University

A Few Words About Me



Jens Teubner

DBIS Group

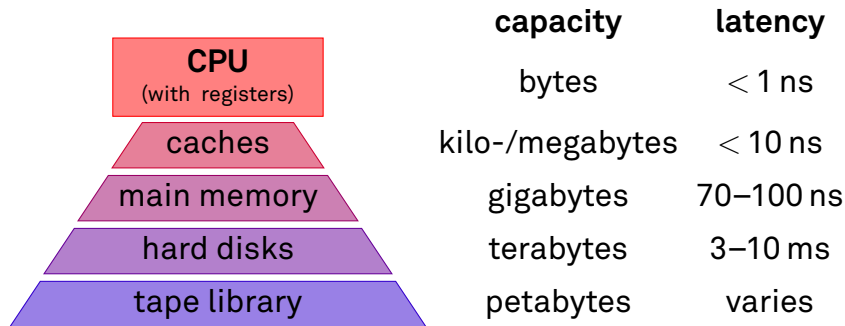
Otto-Hahn-Strasse 14

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Databases and Information Systems Group:

- Databases on modern Hardware
 - in-memory, cache awareness, multi-core
 - data processing on graphics processors (GPUs)
 - data processing on FPGAs (programmable hardware)
- Energy-efficient database software
- Large-scale data processing ($\leadsto$ physics)

Database Folklore (Memory Hierarchy)



RAM vs. disk is like

- Grab the beer in front of you (cheers!) (2 sec)

versus

- Fly to Australia and get it from there (2½ days)

Folklore:

- Avoid disk access **“at any cost”**.
- Use **DRAM to cache disk data**.
 - Database “buffer manager” manages caching.

Hmmm...

- Today’s systems can host terabytes of RAM.

Database Systems with Large Memories

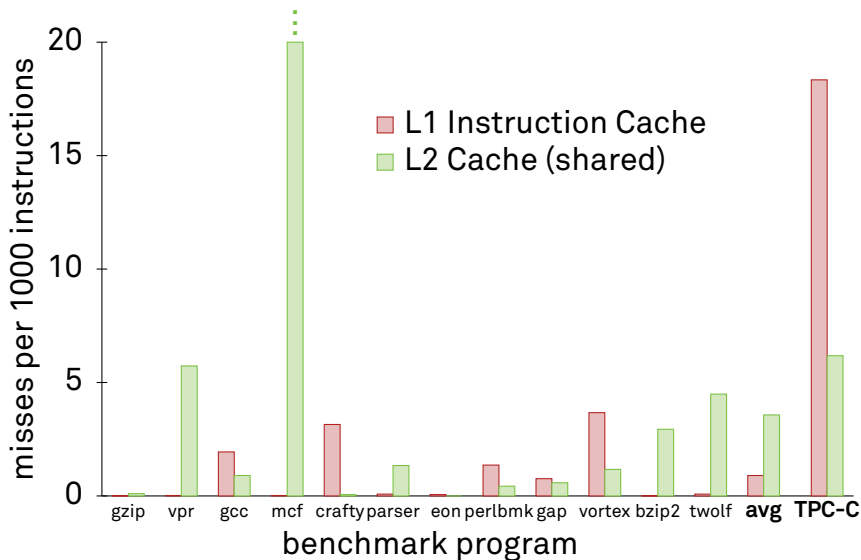
Databases, a concept that had its day?

- Buffer management → overhead
→ “Hidden” behind disk latency in classical systems.
- Transaction management, persistence?

Actually...

- RAM ↔ disk gap → **cache ↔ RAM gap**
- Buffer manager → hardware

Effectiveness of Hardware Caches



**A conventional database
with a large memory
will not do the trick.**

E.g., SAP HANA

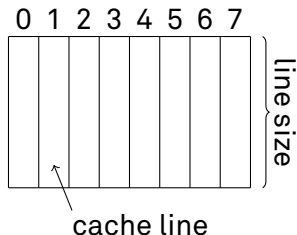
SAP HANA basiert auf der In-Memory-Technologie mit spaltenbasierter Datenspeicherung, die die Vorteile der Multi-Core-Verarbeitung und des SIMD-Instruktionssatzes (Single Instruction, Multiple Data) optimiert. Die Plattform ist vollständig kompatibel mit den Anforderungen des ACID-Standards (Atomarität, Konsistenz, Isolation und Dauerhaftigkeit). Mit intuitiven Modellierungswerkzeugen, Entscheidungsta-

- column-oriented storage?
- multi-core processing?
- SIMD instruction sets?

How CPU Caches Work

For high speed, the **overhead** of caching must be kept low.

- Organize cache in **cache lines**.
- Only load/evict **full cache lines**.
- Typical **cache line size**: 64 bytes.



- Block-wise transfers are well-supported by DRAM chips.
- Organization in cache lines $\leftrightarrow$ principle of locality

Database $\leftrightarrow$ Cache Interaction

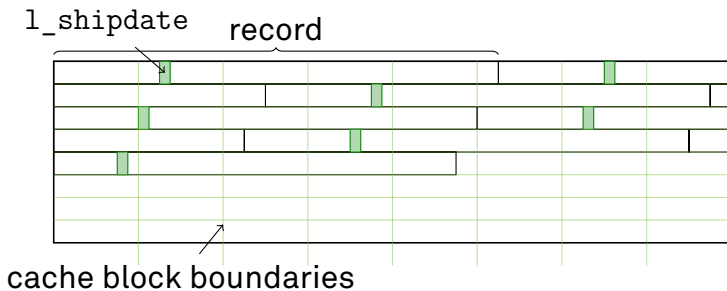
Consider, e.g., a selection query:

```
SELECT COUNT(*)  
  FROM lineitem  
 WHERE l_shipdate = "2009-09-26"
```

- This query typically involves a **full table scan**.

Table Scans and Caches

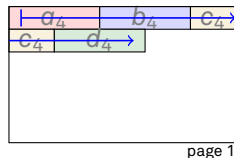
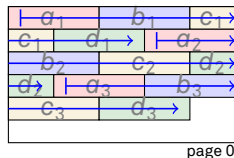
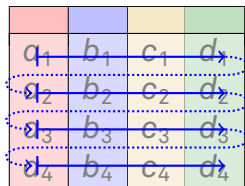
Tuples: **records** stored sequentially on a database page.



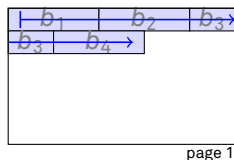
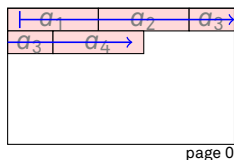
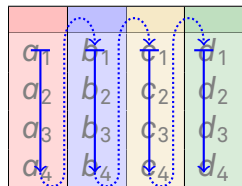
- With every access to a `l_shipdate` field, we load a large amount of **irrelevant** information into the cache.
- 4 bytes for `l_shipdate`, 64 bytes cache line size
→ 94 % garbage fetched!

Row-Wise vs. Column-Wise Storage

This is when we assume **row-wise** storage (also: n -ary storage model, NSM).



Column-wise storage (decomposition storage model, DSM):



...

Column Stores in Commercial DBMSs

Commercial databases have added column-store functionality to their engines:

- **Microsoft SQL Server:**

- Represented as “Column Store Indexes”
- Available since SQL Server 11
- see Larson *et al.*, SIGMOD 2011

- **IBM DB2:**

- IBM DB2 “BLU Accelerator”, a column store that ships with DB2 10.5.
- BLU stands for “Blink Ultra”; Blink was developed at IBM Almaden (↗ Raman *et al.*, *ICDE 2008*).

**Why aren't all databases
built as row stores then?**

MonetDB: Binary Association Tables

MonetDB makes this explicit in its data model.

- All tables in MonetDB have two columns (“head” and “tail”).

oid	NAME	AGE	SEX	→	oid	NAME	oid	AGE	oid	SEX
o ₁	John	34	m		o ₁	John	o ₁	34	o ₁	m
o ₂	Angelina	31	f		o ₂	Angelina	o ₂	31	o ₂	f
o ₃	Scott	35	m		o ₃	Scott	o ₃	35	o ₃	m
o ₄	Nancy	33	f		o ₄	Nancy	o ₄	33	o ₄	f

- Each column yields one **binary association table (BAT)**.
- **Object identifiers** (oids) identify matching entries (BUNs).
- Oftentimes, oids can be implemented as **virtual oids** (voids).
 - Not explicitly materialized in memory.

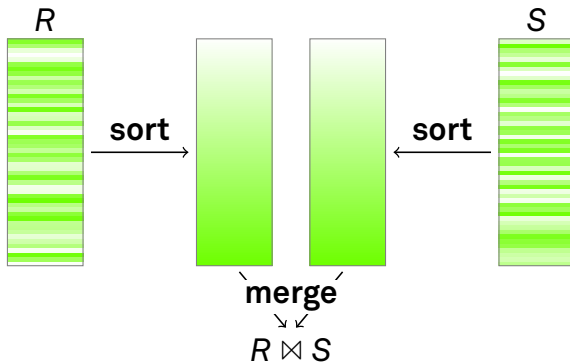
Binary Association Tables

Simplicity of two-column setting → **aggressive optimization.**

Example: `batval_int_add(···)` (i.e., `[+](int, BAT[any, int])`)

```
⋮
if (vv != int_nil) {
    for (; bp < bq; bp++, bnp++) {
        REGISTER int bv = *bp;
        if (bv != int_nil) {
            bv = (int) OP(bv, +, vv);
        }
        *bnp = bv;
    }
} else {
    for (; bp < bq; bp++, bnp++) {
        *bnp = vv;
    }
}
⋮
```

Sort-Merge Join



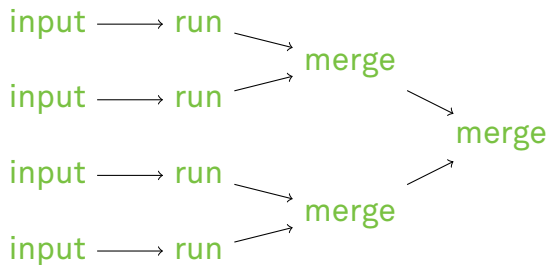
- ✓ Can be done as **external sort**
- ✓ $\mathcal{O}(N \log N)$

Sorting in Databases

The critical part of sort-merge join is **sorting**.

- Method of choice: **merge sort**

- two parts: **run generation** and **merging**

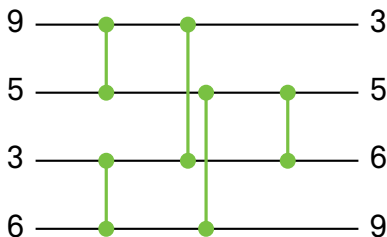


- Both are good candidates for **SIMD acceleration**

Sorting networks

→ **branch free**, supports **data parallelism**

E.g., network for four elements (“even-odd network”):



→ Build larger networks by **merging** sorted runs.

SIMD instructions

E.g., four words per SIMD register:

a_1	a_2	a_3	a_4	xmm0
-------	-------	-------	-------	------

b_1	b_2	b_3	b_4	xmm1
-------	-------	-------	-------	------

$\max(a_1, b_1)$	$\max(a_2, b_2)$	$\max(a_3, b_3)$	$\max(a_4, b_4)$	$\swarrow$
------------------	------------------	------------------	------------------	------------

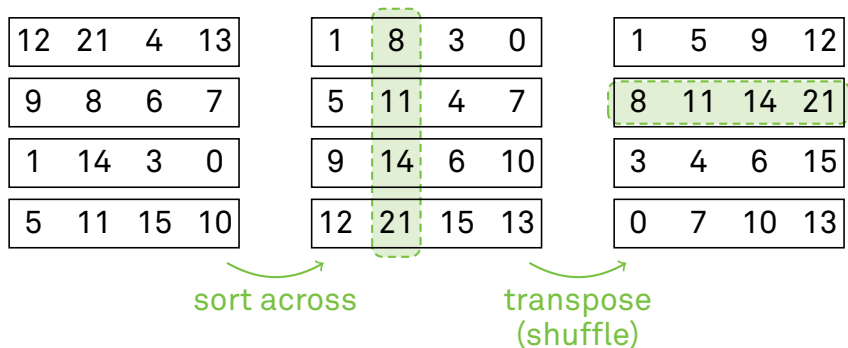
`simd_max(xmm0, xmm1)`



Operations **across** registers, **not within**

→ **But:** Can **shuffle** across and within

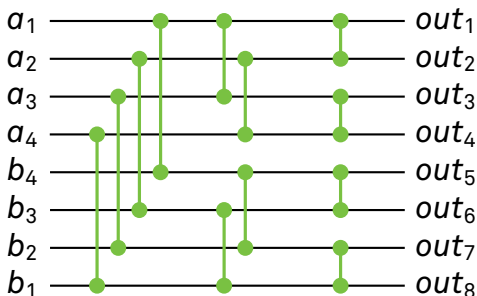
Run generation



- 10 min/max, 8 shuffle, 8 load/store
- 64 bytes in, 64 bytes out (128-bit SIMD)

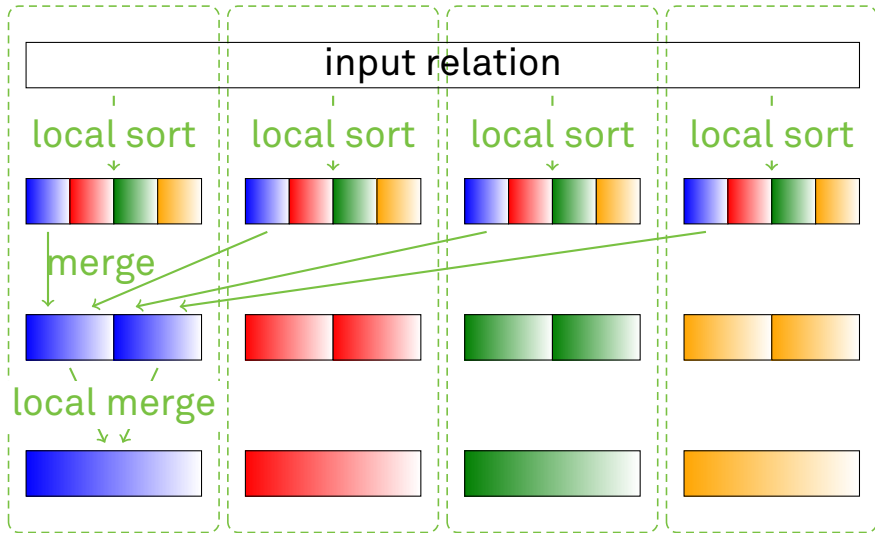
Merging

Two sorted runs, four items each:

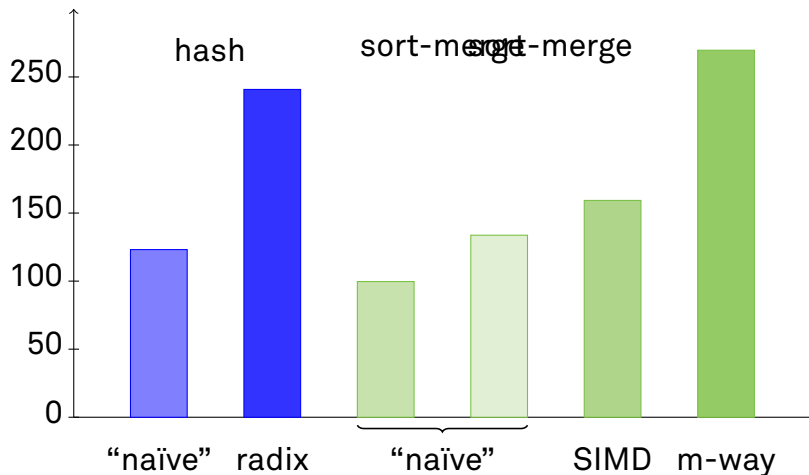


- Input: two SIMD registers **a** and **b**, sorted
- 6 min/max, 10 shuffle, 4 load/store

Sorting and NUMA



Sort or Hash?



■ 12.8 GB $\bowtie$ 12.8 GB

■ Intel E5-4640 (“Sandy Bridge”), 2.4 GHz, 32 cores

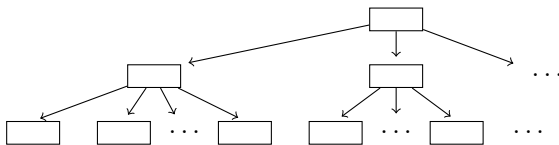
fast in-memory processing
high degrees of hardware parallelism



increased **concurrency** in the system
correctness? scalability?

E.g., B-Trees

B-trees are **the** indexing mechanism used in databases today.



Challenge:

- Update operations may change **structure** of the B-tree.
- Concurrent transactions must not see inconsistent tree.

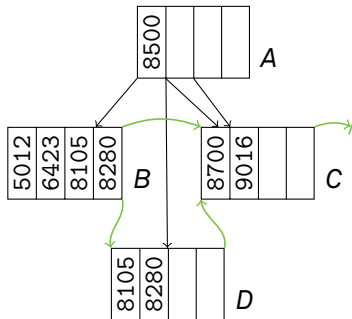
Defensive solution:

- Generously **lock** (“latch”) parts of the tree.

Blink-Trees: “Single-Latch B-Trees”

B-tree variant with **sibling pointers**.¹

- 1 latch & read page *B*;
- 2 create and latch new page *D*;
- 3 populate page *D*;
- 4 set next pointer *D* $\rightarrow$ *C*;
- 5 un-latch *D*;
- 6 set next pointer *B* $\rightarrow$ *D*;
- 7 adjust content of *B*;
- 8 un-latch *B*;
- 9 latch & read *A*;
- 10 adjust content of *A*;
- 11 un-latch *A*;



→ Lines 9–11 can be deferred to a later time.

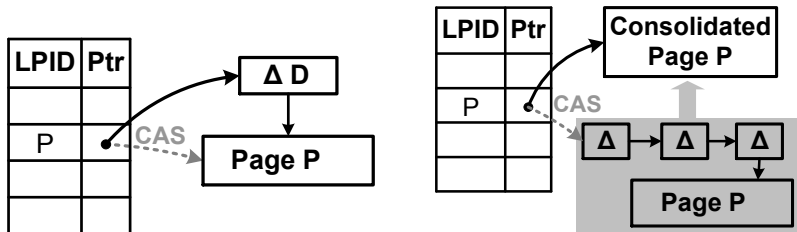
¹PostgreSQL uses Blink-trees.

(Truly) Latch-Free B-Trees?

Avoid latching altogether?

Bw-tree:²

- **Compare-and-swap** instead of latching
- **Delta records** to reduce update volume
- **Logical addressing** to update nodes atomically.



²Levandowski *et al.* The Bw-Tree: A B-tree for New Hardware Platforms. ICDE 2013.

- Implementation heavily optimized ($\leadsto$ caches).
- Part of Microsoft SQL Server (“Hekaton”).
- Ready for **flash-based storage**.
- Ready for **non-volatile memories**.

“In-Memory Databases”

- **Not** just a database and a large RAM!
- Software tailored toward
 - memory/cache efficiency
 - CPU efficiency (including SIMD, etc.)
 - hardware parallelism
 - ...

Specifically, I discussed

- cache awareness → **column stores**
- CPU efficiency → **SIMD, multi-core, NUMA**
- concurrency → **latch-free indexing, Bw-tree**